

Asian Institute of Technology

Digital Integrated Circuit Design

Rationale: To provide fundamental concepts in digital systems design. To provide a basic understanding of some computer-aided techniques used in the design verification, synthesis, optimization, and implementation of digital systems.

Catalog Description: Digital Systems Design Process and CAD Tools. Combinational and Sequential Circuits Design and Implementation. Input/Output Design and Clock Generation. Design of Memory. Hardware Description Language (HDL). Rapid Prototyping and Implementation of Digital Systems. Memory System Design and Test. Testing and Design for Testability (DFT).

Pre-requisite: None

Course Outline:

I Introduction

1. Design of static CMOS, nMOS and BiCMOS inverters
2. Calculation of noise margins, power dissipation and gate delays

II Review of Logic Design Fundamentals

1. Combinational Logic Design
2. Logic Simplification and Synthesis
3. Sequential Logic Design
4. Finite State Machine Design and Implementation

III Design of Combinational Circuits

1. Static CMOS Design
2. Dynamic CMOS Design
3. Power Consumption in CMOS Gates

IV Design of Sequential Circuits

1. Static Sequential Circuits
2. Dynamic Sequential Circuits

V Design of I/Os and Clock Generation

1. I/O Structures
2. PLL, clock generation and clock buffering

VI Design of Memory

1. Memory Core
2. Memory Peripheral Circuits
3. Memory Faults and Test Patterns

VII Digital System Design using Hardware Description Language

1. Introduction to HDL, Modeling and Designing with VHDL
2. VHDL Description of Combinational Networks
3. VHDL Description of Sequential Networks
4. VHDL Model for Memories

VIII Rapid Prototyping and Implementation of Digital Systems

1. Field Programmable Gate Arrays (FPGA), Complex Programmable Logic Devices (CPLD)
2. Logic Synthesis for FPGA and CPLD

IX Testing and Design for Testability (DFT)

1. Boundary-Scan Test
2. Faults & Fault Simulation
3. Automatic Test-Pattern Generation
4. Scan Test & Built-in Self-test

Laboratory Session

- Laboratory 1: Adder and Counter Using VHDL coding
- Laboratory 2: 4bit Adder and 4bit Counter with Test bench and Verification
- Laboratory 3: Traffic Light Design and Implementation
- Laboratory 4: Dice Game Design and Implementation
- Laboratory 5: Traffic Light Implementation to FPGA
- Laboratory 6: Dice Game Implementation to FPGA

Text Books:

J. M. Rabaey:

Digital Integrated Circuits - A Design Perspective, 2nd Ed., Prentice-Hall, 2002

N. Weste and K. Eshraghian:

Principles of CMOS VLSI Design - A Systems Perspective, Prentice-Hall, 1993

References:

C. H. Roth, Jr.:

Digital Systems Design Using VHDL, PWS Publishing Com., 1998

Michael J. S. Smith:

Application-Specific Integrated Circuits, Addison-Wesley, 1997

Journals:

- IEEE Transactions on VLSI Systems
- IEEE Journal of Solid State Circuits
- Kluwer Journal of VLSI Signal Processing
- Taylor and Francis Journal of VLSI Design
- Elsevier journal of Microprocessors and Microsystems
- Elsevier Journal of Microelectronics

Grading System: The final grade will be computed from the following constituent parts: *mid-sem exam (30%), final exam (35%), laboratory experiments (25%) and assignments (10%)*. *Open-book examination is used for both mid-sem and final exam.*

Instructor: Visiting Faculty